（NVIDIA 英伟达）10个硬件岗位任你挑选！

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* Senior CPU Architecture Engineer
* Senior NVDLA Architecture Engineer
* Senior ASIC Design Engineer (Security)
* Senior ASIC Design Engineer (Video)
* Senior Verification Engineer
* SOC Design Engineer
* ASIC Design/Verification Engineer
* ASIC Verification Engineer (Clocks)
* Senior Physical CAD Engineer
* ASIC Physical Design Engineer

我需要如何申请呢？

咨询请致电02938053694

如果你对以上职位感兴趣，请发简历至：Olivialiu@careerintlinc.com

邮件标题：职位名+姓名+毕业时间+可到岗时间 +招聘信息来源

****Senior CPU Architecture Engineer

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* Architect NVIDIA's next generation of RISCV CPU
* Co-work with software team to identify architecture requirements
* Evaluation of different architecture solutions
* Define architecture of the CPU core and various hardware components surrounding the CPU, like local memory, interconnect and crypto accelerators
* Validate the new architecture on CMOD

**What we need to see**

* BS/MS in electrical/computer engineering and related.
* 3+ years’ experience in hardware architecture
* Strong skills in C/C++
* Solid understanding to computer architecture

**Ways to stand out from the crowd**

* Project experiences of complex CPU architecture
* Knowledge or project experiences of RISCV CPU
* Knowledge of project experiences on SystemC modeling
* Broad understanding to computer security and crypro algorithms like AES/SHA/RSA/ECC
* Fluent English (both written and spoken) and excellent communication skills
* Demonstrated ability to work independently as well as in a multi-disciplinary group environment

Senior NVDLA Architecture Engineer****

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* Building next generation of NVDLA for both internal usage and open source
* Work on Deep-Learning architecture, algorithms, and software development
* Develop function/performance/power models for NVDLA
* Co-work with other HW team to deliver high quality Deep-Learning processors.

**What we need to see**

* MS/Ph.D in electrical/computer engineering and related.
* 3+ years strong experience in algorithm/architecture development in one or some of the following technologies: CPU, GPU, DSP, deep-learning processor, Image Processor.
* Solid software skills in C/C++

**Ways to stand out from the crowd**

* Hardware design or driver development background is a plus.
* Fluent English (both written and spoken) and excellent communication skills
* Demonstrated ability to work independently as well as in a multi-disciplinary group environment

****Senior ASIC Design Engineer(Security)

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* Building NVIDIA's next generation of RISCV security CPU
* Co-work with architect team to define CPU architecture/micro-architecture
* Design and verification of various hardware modules including CPU core, interconnect, and various peripherals including DMA, AES, SHA, RSA and ECC engines

**What we need to see**

* BS/MS in electrical/computer engineering and related.
* 3+ years’ experience in ASIC design. Strong design/implementation skills in Verilog. Solid understanding in timing/power optimization skills of digital design

**Ways to stand out from the crowd**

* Solid understanding to computer architecture
* Project experiences of complex CPU architecture or micro-architecture design like out-of-order or dual-issue cores
* Knowledge or project experiences of RISCV CPU
* Broad understanding to computer security and crypro algorithms like AES/SHA/RSA/ECC
* Perl scripting skills is appreciated as a plus.
* Fluent English (both written and spoken) and excellent communication skills
* Demonstrated ability to work independently as well as in a multi-disciplinary group environment

****Senior ASIC Design Engineer(Video)

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* Building NVIDIA's next generation of video codec engines
* Co-work with video architect to define video architecture/micro-architecture
* Design and verification of video hardware module.

**What we need to see**

* BS/MS in electrical/computer engineering and related.
* 3+ years ‘experience in ASIC design. Strong design/implementation skills in Verilog. Solid understanding in timing/power optimization skills of digital design

**Ways to stand out from the crowd**

* Broad knowledge with video and image processing techniques and with digital video compression standards such as H.264, H265, VP9 and AV1 is a big plus.
* Knowledge with computer vision algorithms like optical flow and stereo is a plus.
* Familiar with HLS tool, like Mentor Catapult
* Perl scripting skills is appreciated as a plus.
* Fluent English (both written and spoken) and excellent communication skills
* Demonstrated ability to work independently as well as in a multi-disciplinary group environment

****Senior Verification Engineer

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* You will participate in the research of verification methodology to improve automation and productivity to produce Nvidia’s new high-quality state of the art products.
* Read IAS and design specs to understand the design requirement and build corresponding testplan. Review the testplan with arch/design engineers.
* You responses to build block/IP testbench based on UVM methodology.
* The responsibilities includes building test run and regression flow. Triage failures in regression and help designer root cause the bug.
* Work includes Build various metrics (passing rate, functional coverage, etc) and monitor its health.
* Take SOC verification on fullchip test environment for IPs
* Analyse functional/code coverage result and identify the coverage holes. Work with design engineer to improve the coverage score.
* Deploy the advanced verification methodology and infrastructure of the SOC/IP

**What we need to see**

* BS / MS in electrical / computer engineering and related.
* 3+ years (MS) or 5+ years (BS) working experience.
* Familiar with advance verification methodology (UVM, VMM, OVM, etc), tools and flow
* Fully experienced verification flow, including testplan, test, coverage model, testbench, BFM modeling.
* Deep understanding in Verilog and HVL (High-level Verification Language)

**Ways to stand out from the crowd**

* Strong programming skills in Perl and C/C++is plus
* Having good arch/design experience is big plus.
* At least good at one of the script programing lanange : Perl, Shell, Ruby, Python, etc.
* Fluent English (both written and spoken) and excellent communication skills
* Proven ability to work independently as well as in a multi-disciplinary group environment
* Strong analytical skills

****SOC Design Engineer

**工作地点：上海 浦东新区 秋月路26号**

The NVIDIA System-On-Chip (SOC) group is looking for a top SOC engineer with an interest in RTL integration and design as well as verification. The ideal candidate for this position has great passion for methodologies and automation solutions that enable creating SOCs in the least amount of time.

In this position, you will have the opportunity to be responsible for creating complex GPUs and SOCs and interface directly with unit-level, Physical Design, CAD, Package Design, Software, DFT and other teams. Additionally, you will be involved with defining and creating methodologies that create more efficient and flexible SOCs in future.

**What we need to see**

1. BS or MS (preferred) in EE or CS
2. Understand frontend ASIC design/verification/implementation flow
3. Excellent analytical and problem-solving skills
4. Strong coding skills in Perl or other industry-standard scripting languages
5. Fluent English (both written and spoken) and excellent communication skills to interface with many groups and build consensus
6. Good team work spirit, easy to cooperate with team members
7. Prior experience in implementing System-On-Chip is a plus
8. Prior experience in RTL build and design automation is a plus

****ASIC Design/Verification Engineer

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* Micro-architecture definition for System-level modules (Reset, Fuse, Strap, In-silicon measurement, Floorsweep, etc…)
* RTL design, synthesis, timing and silicon bring-up
* Unit-level and System-level verification
* Chip level integration

**What we need to see**

* BS / MS in electrical / computer engineering and related.
* Familiar with verification methodology, tools and flow
* Understand frontend ASIC design flow including RTL design, synthesis and timing analysis
* Excellent analytical and problem-solving skills
* Broad knowledge with Video techniques, SOC architecture and Computer architecture is a big plus
* Strong programming skills in C/C++ and Perl is appreciated as a plus
* Fluent English (both written and spoken) and excellent communication skills
* Good team work spirit, easy to cooperate with team members

****ASIC Verification Engineer (Clocks)

**工作地点：上海 浦东新区 秋月路26号**

NVIDIA Clock team is now looking for ASIC engineers with strong logic design or verification background. In this position, you will take part in all stages to design modern complex GPU chips with state-of-art features and flows. To implement various functions, you will work directly with different global teams, as ARCH/SW, ASIC Design, CAD, Package, DFT and Physical Design teams. Additionally, you will be involved in defining and creating methodologies that create more efficient and flexible SOCs in future.

**What you'll be doing**

* Module-level or Chip-level logic design, synthesis, timing constraints, and silicon bring-up.
* Module-level or Chip-level verification, both for function and test mode
* Methodology or Flow development for above tasks.

**What we need to see**

* BS / MS in electrical / computer engineering and related.
* Understand ASIC design/verification/implementation flow
* Familiar with design/verification languages as C/C++, Verilog or VHDL
* Know industrial standard scripting language as Perl, or Python, TCL, Ruby
* Excellent analytical and problem-solving skills
* Fluent English and excellent communication skills
* Good team work spirit, easy to cooperate with team members
* Understand JTAG, DFT, or OCC is a plus

****SeniorPhysical CAD Engineer

**工作地点：上海 浦东新区 秋月路26号**

**What you'll be doing**

* Develop the physical design flow and methodology for all chips in NVIDIA (including GeForce®/Tegra™/Tesla™/Quadro™).
* Work with EDA vendors on tools evaluation and improvement.
* Develop inhouse tools and solutions.
* Support the global physical design team.

**What we need to see**

* BS/MS in CS/EE/ME.
* Experiences in one of the following areas: Floorplan, Place&Route, STA, layout DRC/LVS, DFT, circuit design, RTL.
* Strong programming capabilities.

**Ways to stand out from the crowd**

* Proficiency in Perl, TCL, Shell.
* Experiences in VLSI design automation or methodology.
* Knowledge on EDA tools: Synopsys (ICC/DC/PT/STAR-RC/Astro/PC/Talus), Cadence (SOCE), Mentor Graphics (Pinnacle/Olympus) etc.

****ASIC Physical Design Engineer

**工作地点：上海 浦东新区 秋月路26号**

We are now looking for an ASIC PD Engineer.

**What you'll be doing**

* Chip integration and netlist generation
* Synthesis
* Netlist quality check
* Formal Verification
* Constraints creation and validation, timing budget.
* Co-work with PR engineers to implement chip partition and floorplan
* Work in conjunction with RR engineers to achieve timing closure for both partition and full chip level
* Achieve special timing closure, such as io, test, clock etc.
* Function eco creation
* Develop and enhance entire timing closure flow from frontend (pre-layout) to backend (post-layout)
* Flow automation development
* Methodology in any of above areas.

**What we need to see**

* BSEE, MSEE is preferred
* Project experience in IC design implementation
* Courses taken in circuit design, digital design
* Hand-on experience in EDA software from Synopsys (DC/PT/Formality), Cadence (LEC) is preferred
* Ways to stand out from the crowd:
* Proficient user of Perl or TCL is preferred
* Excellent English communication skill